Method for providing an Area Optimized Binary Orthogonality Checker

ABSTRACT OF THE DISCLOSURE

[0037] A method for minimizing the area of a binary orthogonality checker implemented in static CMOS circuits for minimizing the gate count and area needed for checker implementation. The method is adaptable to various libraries of logical gates to implement the circuit and the area for each gate in the library. The optimal mix of hierarchical levels and stages is determined such that the orthogonality checker achieves the minimized circuit area. An orthogonality checker is employed in a scalable selector system for controlling data transfers and routing in a data processing system to allow. Combining orthogonality checking with existing selector hierarchically allows for the maximum reuse of circuits, signals, and proximity; thus potentially reducing wiring as well. Multiple hierarchical checks are used in favor of one large. This structure is extended to multiple hierarchical levels and works with orthogonality checks of any size or implementation. The invention also determines the optimal hierarchical structure for a given technology library and a given number of inputs to check. It can also be used within a flat hierarchy or macro as a technique to reduce circuits.